



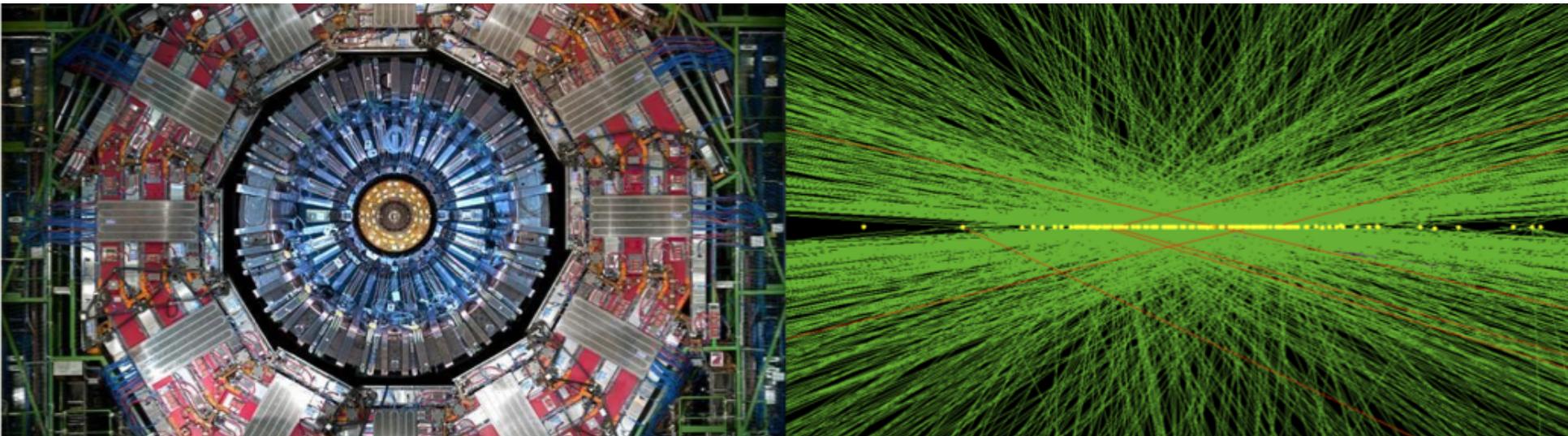
P04

Outcome of Technical Review and Recent Progress

David Stuart, UC Santa Barbara

Fermilab Director's Review

19 March 2019





Outline

- Outcome of the MTD Technical Review
- Recent Technical Progress
 - Optimized BTL crystal geometry
 - Design of BTL Concentrator Card
 - R&D for BTL SiPMs
 - Design of ETL Readout ASIC
 - Design of ETL module assembly
- Summary



MTD Technical Review 15-16 Nov.

Technical Review committee:

Jarek Kaspar, U. Washington

Mitch Newcomer, U. Pennsylvania

Mark Oreglia, U. Chicago

Rob Roser, Fermilab (chair)

Charged to assess physics requirements, technical design and its maturity, R&D plan, organization and risks, and documentation (CDR).

Committee's report is positive on all charge items.

Committee provided specific recommendations:

Technical Review recommendations

- ✓ ETL-R1: It is crucial to follow the schedule of beam test and/or system integration tests to verify functionality of the LGAD/ROC/Back-end systems
- We are planning a series of tests aimed at each major development stage
 - Will examine the mechanical, thermal, and electrical performance of modules
 - Will use realistic backend electronics as it becomes available
 - Test full sensor-to-DAQ chain with multiple modules
 - Beam tests to verify the production modules.

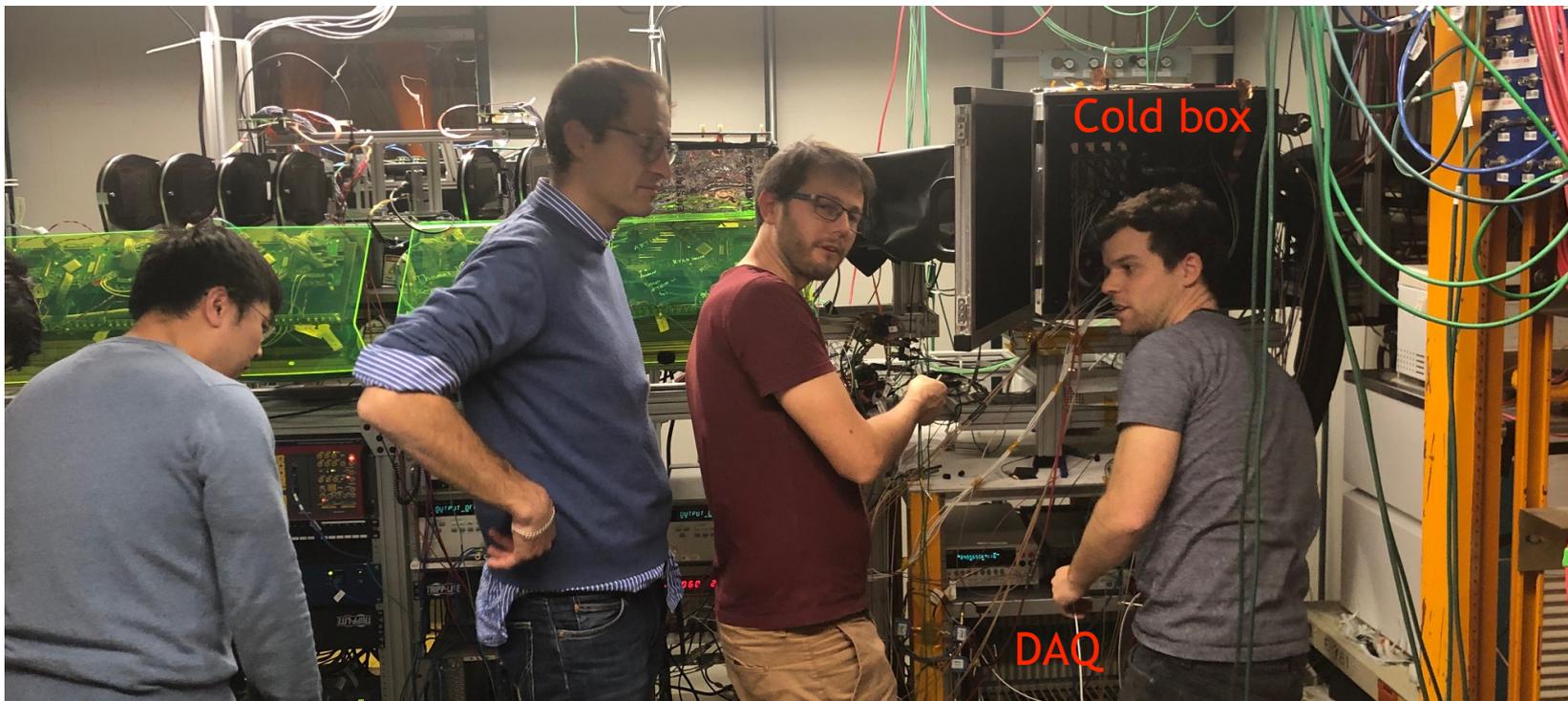
Technical Review recommendations

- ✓ BTL-R1: It is crucial to follow the schedule of beam test and/or system integration tests to verify functionality of the readout unit and compatibility with the other systems.
- Initial beam and system tests planned with sensor-loaded readout units
 - Continue these tests through to final prototype, pre-production, and production stages.

Technical Review recommendations

✓ ETL & BTL: It is crucial to follow the schedule of beam test and/or system integration tests...

Series of dedicated test beams planned, and we are also now running in a long term, parasitic-mode at FTBF, with devices left downstream in cold box.



Si Xie (Caltech), Paolo Meridiani (Rome), Marco Lucchini (Princeton), and Ryan Heller (FNAL) in the Fermilab test beam



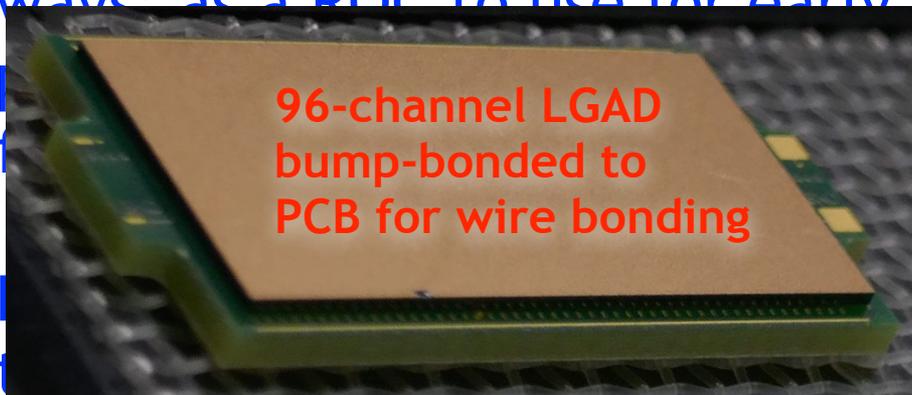
Technical Review recommendations

- ✓ ETL-R2: Identify alternative ASIC solutions from existing or potentially viable prototypes of other systems, and create a decision matrix for breakpoints in the ETLROC development in case that device falls behind in the development schedule or fails to function as required.
- Potential use of alternative ASIC solutions comes in two ways: as a ROC to use for early sensor and module prototyping, and as a ROC to use for production of the final detector.
- For early prototyping, we have designed test boards using the SKIROC2 ASIC to read out large prototype LGAD sensors and test bump-bonding performance with sensors bonded to interposers.

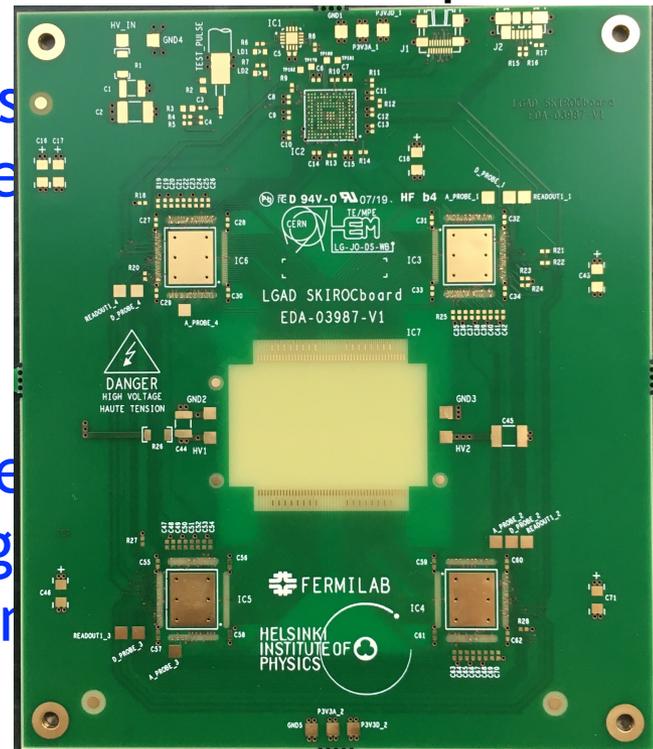
Technical Review recommendations

✓ ETL-R2: Identify alternative ASIC solutions from existing or potentially viable prototypes of other systems, and create a decision matrix for breakpoints in the ETLROC development in case that device falls behind in the development schedule or fails to function as required.

- Potential use of alternative ASIC solutions ways: as a ROC to use for early se



- and test bump-bonding performance to interposers.



SKIROC2-CMS based readout board, modified from HGCAL test boards



Technical Review recommendations

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- Potential use of alternative ASIC solutions comes in two ways: as a ROC to use for early sensor and module prototyping, and as a ROC to use for production of the final detector.
- Considering use of the ATLAS HGTD ALTIROC prototypes.
 - Discussed with HGTD PM and plan for shared testing.
 - Close collaboration on sensor prototyping in beam tests.



Technical Review recommendations

- ✓ ETL-R2: Identify alternative ASIC solutions from existing or potentially viable prototypes of other systems, and create a decision matrix for breakpoints in the ETLROC development in case that device falls behind in the development schedule or fails to function as required.
- For the production phase, the ALTIROC could be a viable alternative if it meets our specs for power and time resolution for small signals and it turns out that the ETL ROC does not.
- Discussions between design teams have shared progress, and the results from the 1st ALTIROC prototype informed the improvements implemented in the ETL ROC design.
- We will continue these discussions, and feedback will help optimize each of the designs for their respective needs and mitigate risks.
- If either encounters functional problems, these discussions will ease cross-adoption of designs.
- Decision points are set by the prototyping schedule; the first ETL ROC prototype with all stages will be measured next year.

Technical Review recommendations

- ✓ ETL-R3: Identify criteria for acceptable SEE rates in the ETLROC and possible error mitigation schemes.
- Corruption of data bits has a negligible effect.
- For configuration bits, we are incorporating the standard Triple Modular Redundancy approach.
- Correlated effects are suppressed by separating replicas spatially; investigating time delays for further suppression.
- To correct bit flips, we will use RD53 “trickle reconfiguration”
- Impact on efficiency will be simulated to specify the criteria, and we are considering ways to measure rates with ion beams



Technical Review recommendations

- ✓ BTL-R3: Consider setting granularity of number of chips/card so that one DC-DC converter is matched to a single TOFHIR readout card.
- The current design incorporates this by assigning a single DC-DC converter per TOFHIR readout card, with another two converters used to power the Concentrator Card.

Technical Review recommendations

- ✓ BTL-R4: Develop a plan for powering up the ASICs cards connected to the concentrator card and for exploiting the lpGBT capabilities for control and environmental monitoring.
- We are developing a powering plan using the GBT SCA output pins to control enabling of each DC-DC converter.
- The GBT SCA inputs will be used to monitor
 - the power status
 - input and output voltages
 - concentrator card temperature
 - SiPM temperatures
 - SiPM bias currents



Technical Review recommendations

- ✓ BTL-R2: In P6, identify the external dependencies such as lpGBT, DC-DC converter, and ETH manufacturing of the DC-DC converter board.
- We have a watch list of the external deliverables.
- Included in the P6 schedule with links to the dependent activities.
- Assigned contacts responsible for monitoring their progress.



Technical Review recommendations

✓ R1: Continue on your plan to achieve CD-1 this coming April

- We will.

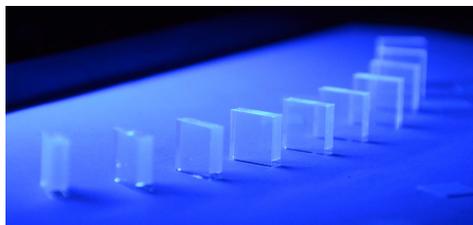
Recent technical progress



Optimization of BTL geometry

- Since TR, we've completed the BTL geometry optimization.
- Studied tile vs bar option.

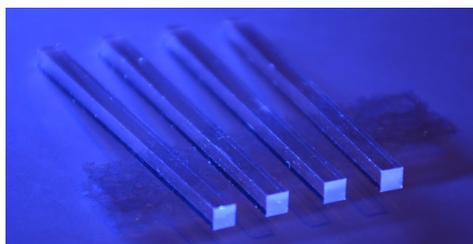
Tiles



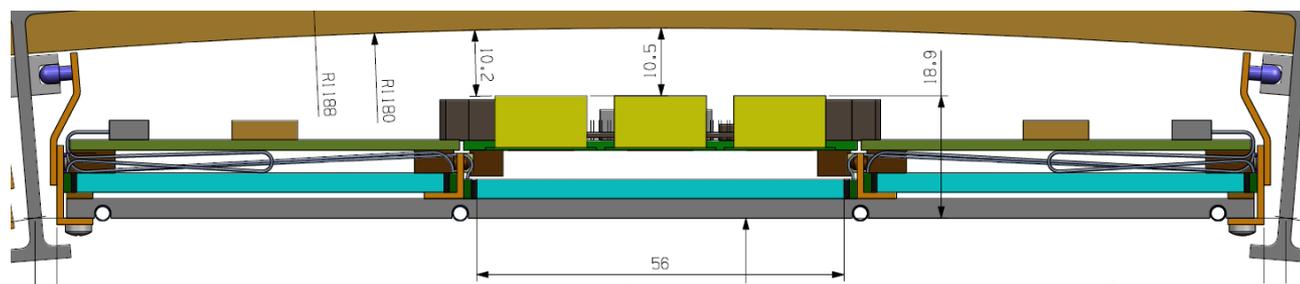
8x8x3 mm



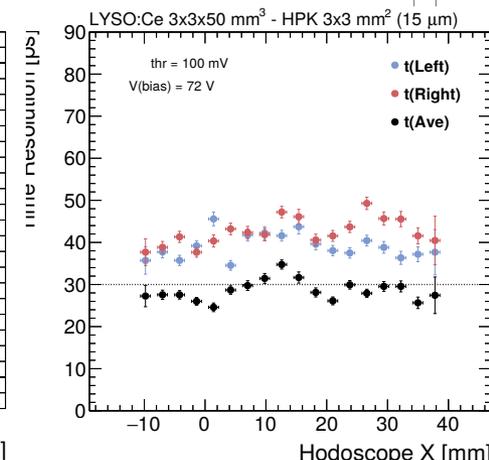
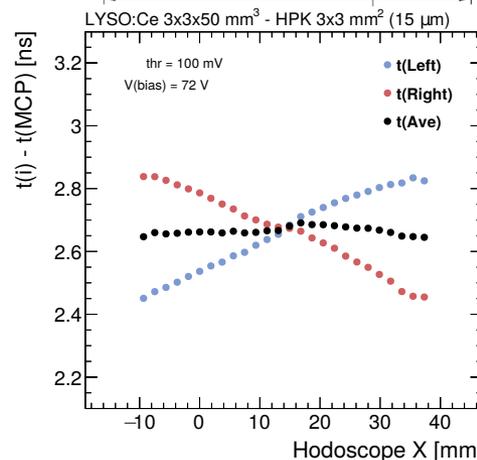
Bars



3x3x57 mm

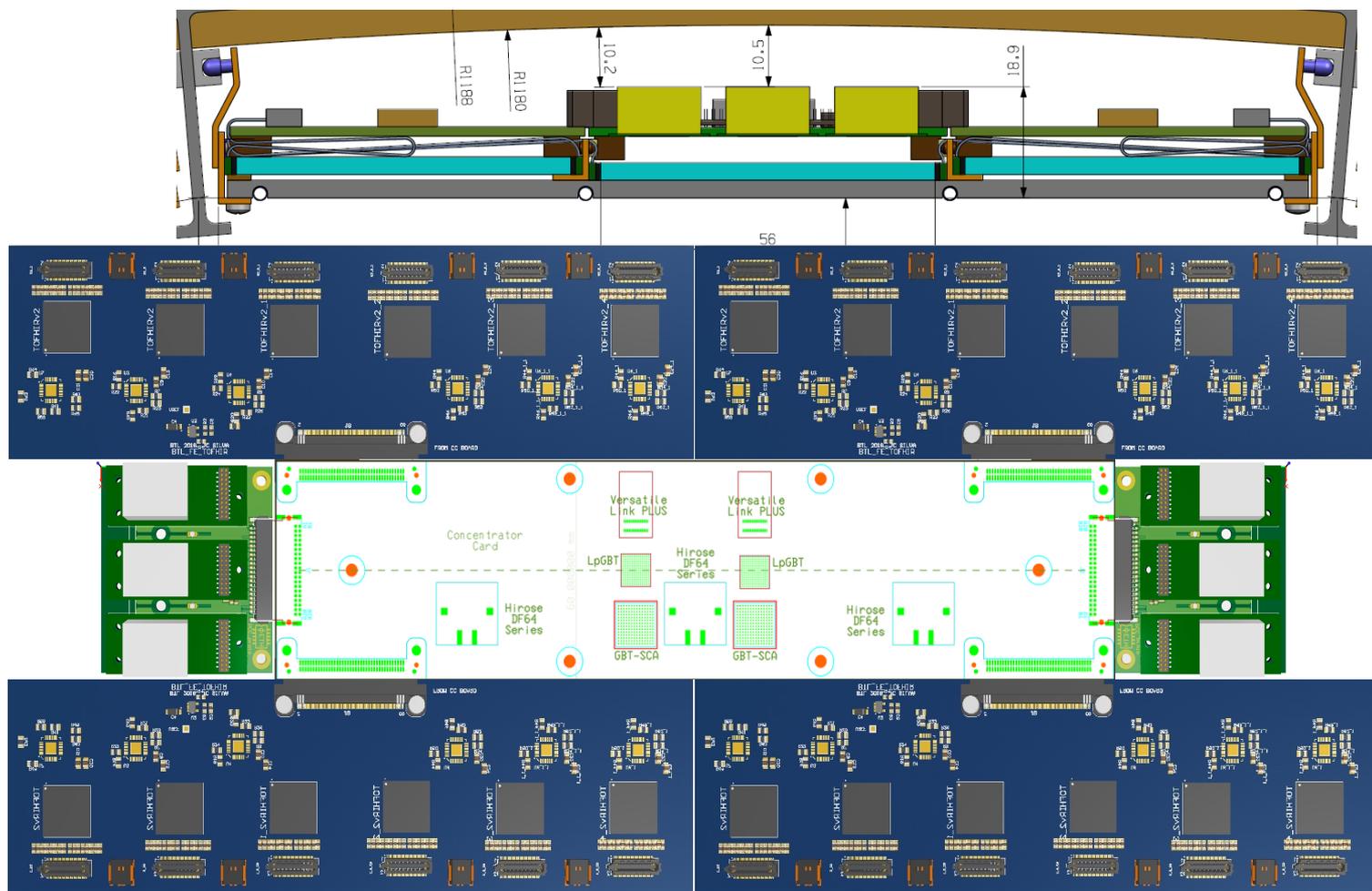


- Bar geometry selected in Dec.
- Two measurements/hit
 - Improved time resolution
 - Uniform time vs position
 - Occupancy increased, but still low.



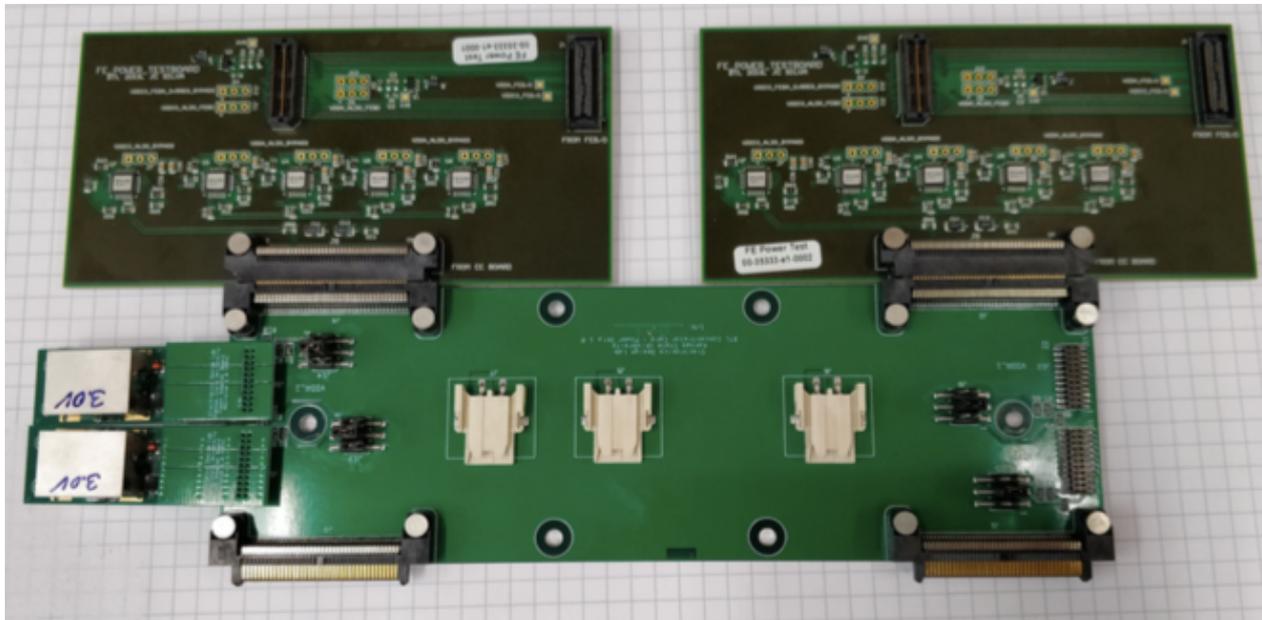
Design of Concentrator Card

- Design and production of concentrator card is a US CMS deliverable; significant progress since last June



Design of Concentrator Card

- Design and production of concentrator card is a US CMS deliverable; significant progress since last June
- Power-only prototype in hand

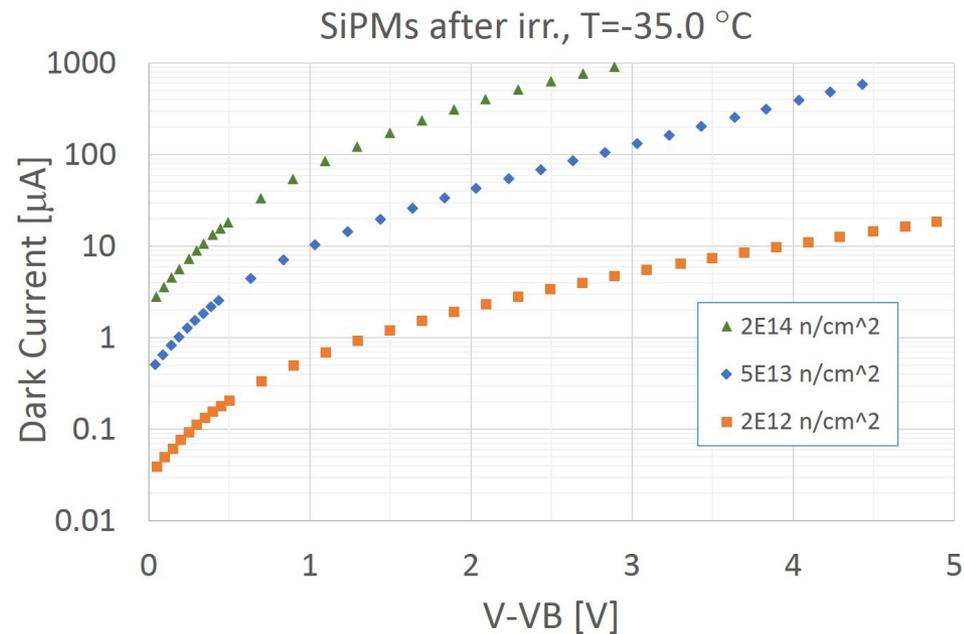
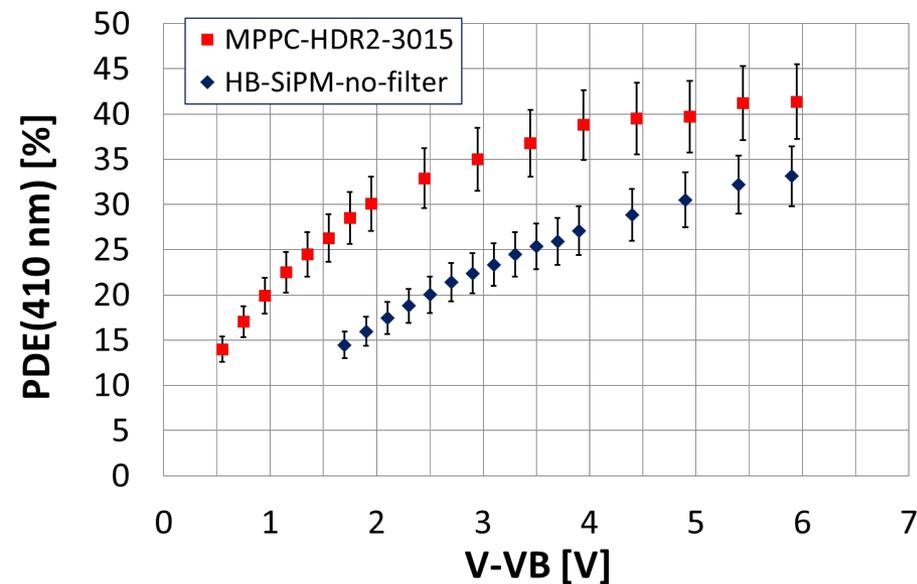


- Prototype this summer.
- Details in Yurii Maravin's talk in tomorrow's breakout.



SiPM R&D

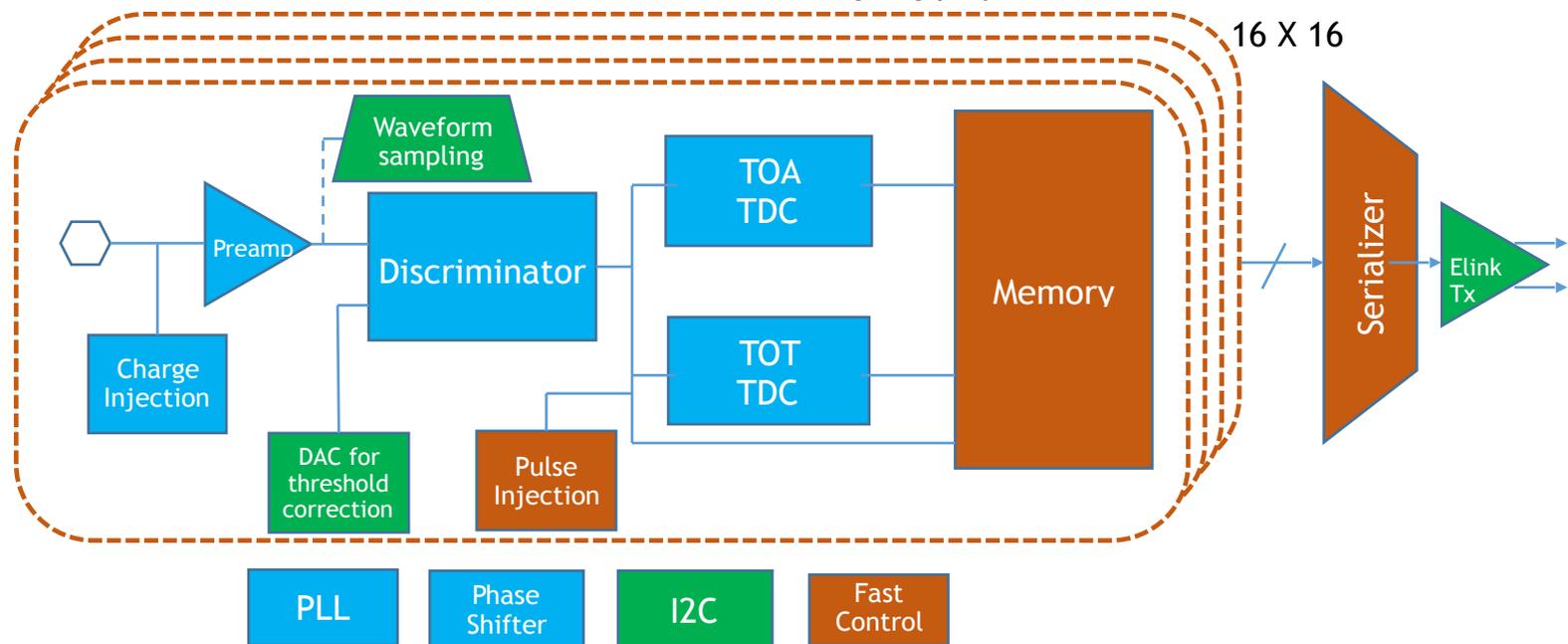
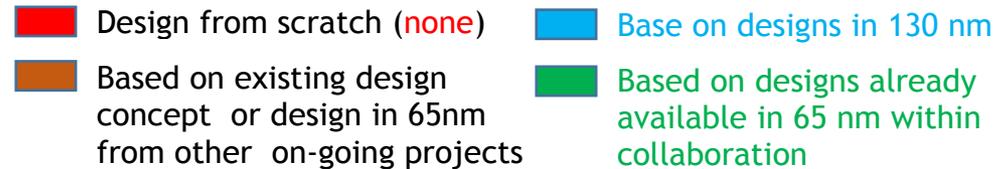
- R&D and procurement of SiPMs is a US CMS deliverable; significant progress since last June
- New devices from HPK and FBK tested before and after irradiation and annealing.



- Details in Mitch Wayne's talk in tomorrow's breakout.

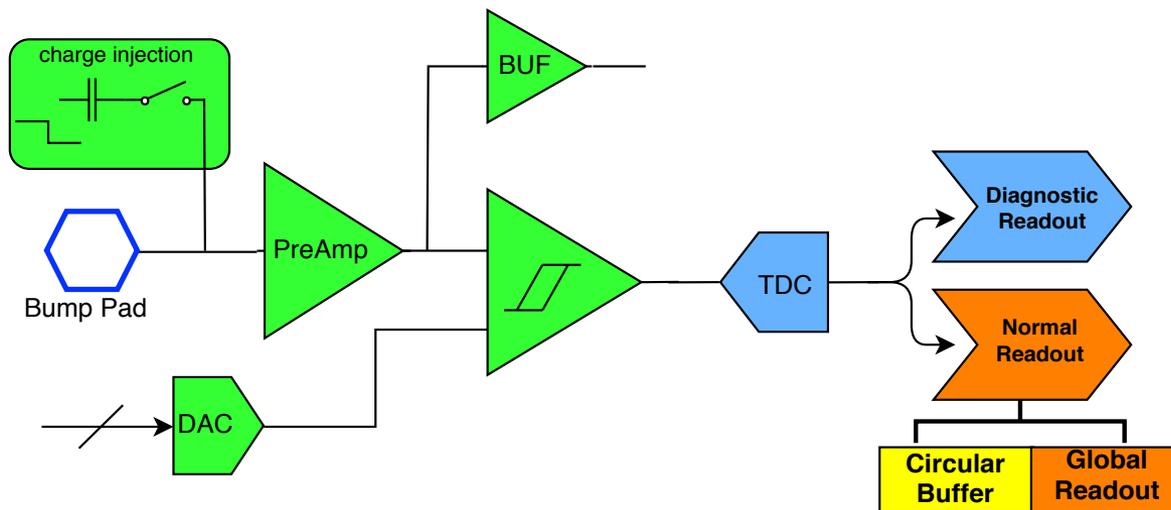
ETL Readout ASIC progress

- Design of the ETL ROC is a significant US CMS deliverable.
- Design challenge is extracting TOA of signals, which can be small (~5 fC) after dose, within constrained power budget.
- ASIC block diagram developed.
- Based on existing IP blocks.

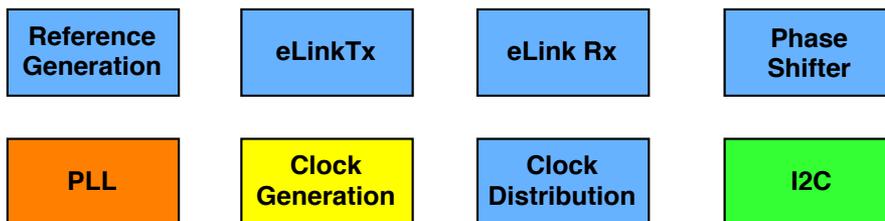
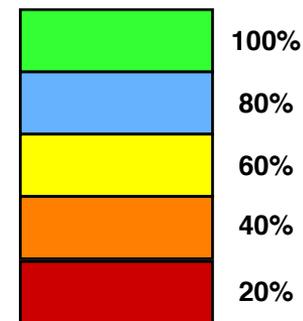


ETL Readout ASIC progress

- Significant progress on design of all building blocks
- Blocks critical to time resolution performance completed.

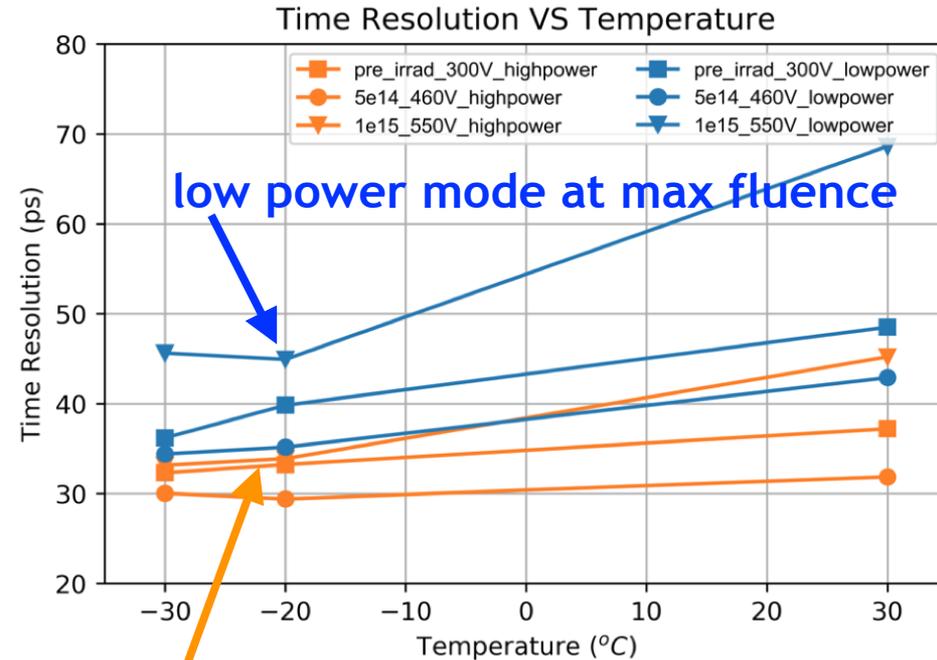
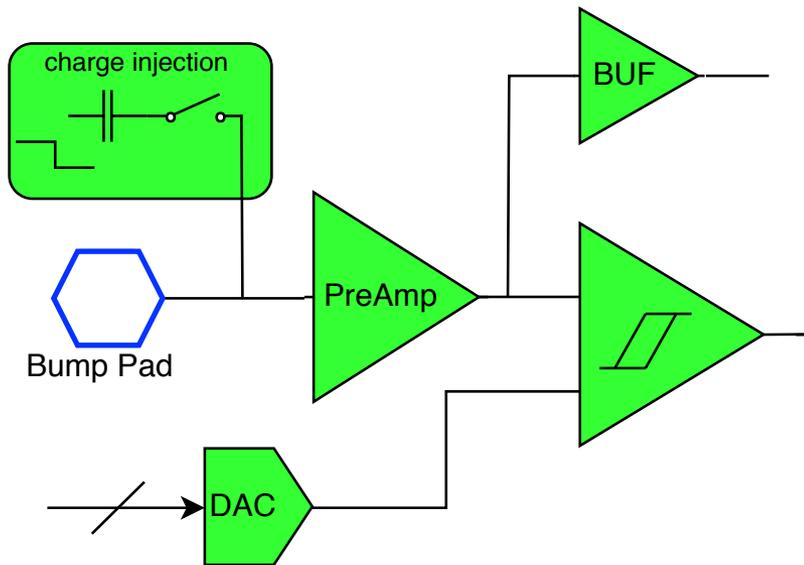


Progress Legend



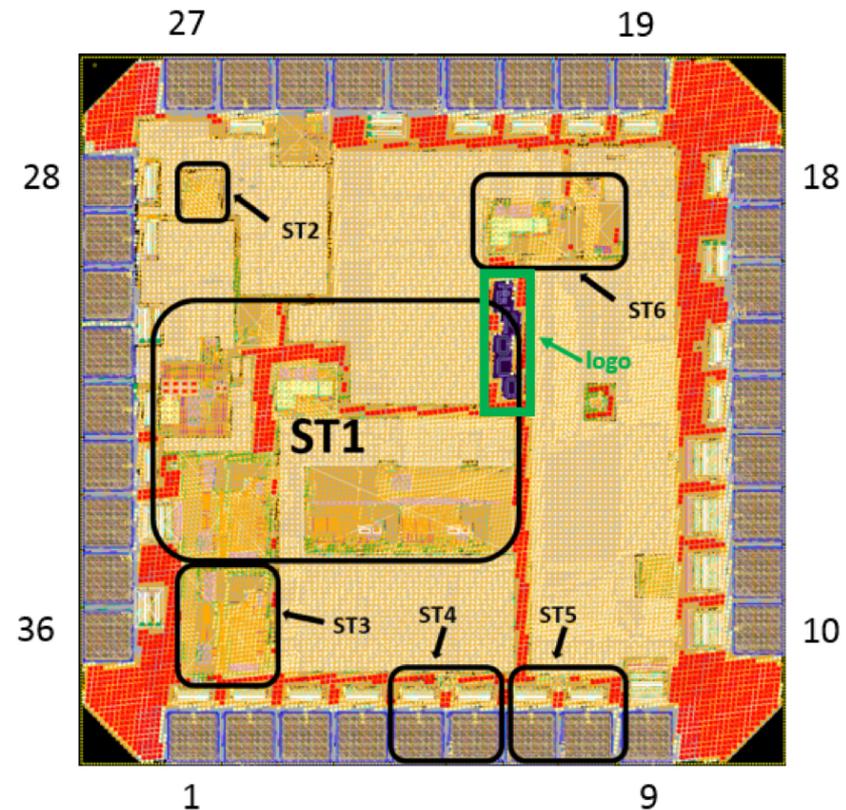
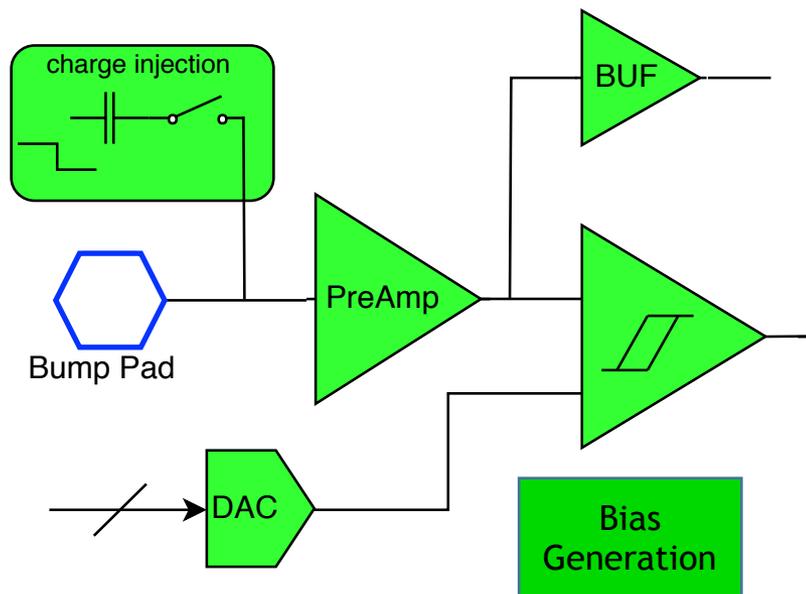
ETL Readout ASIC progress

- Critical preamp + discriminator stages complete and perform well in simulation.
- Meets spec of 50 ps/hit \rightarrow 35 ps / 2-hit track



ETL Readout ASIC progress

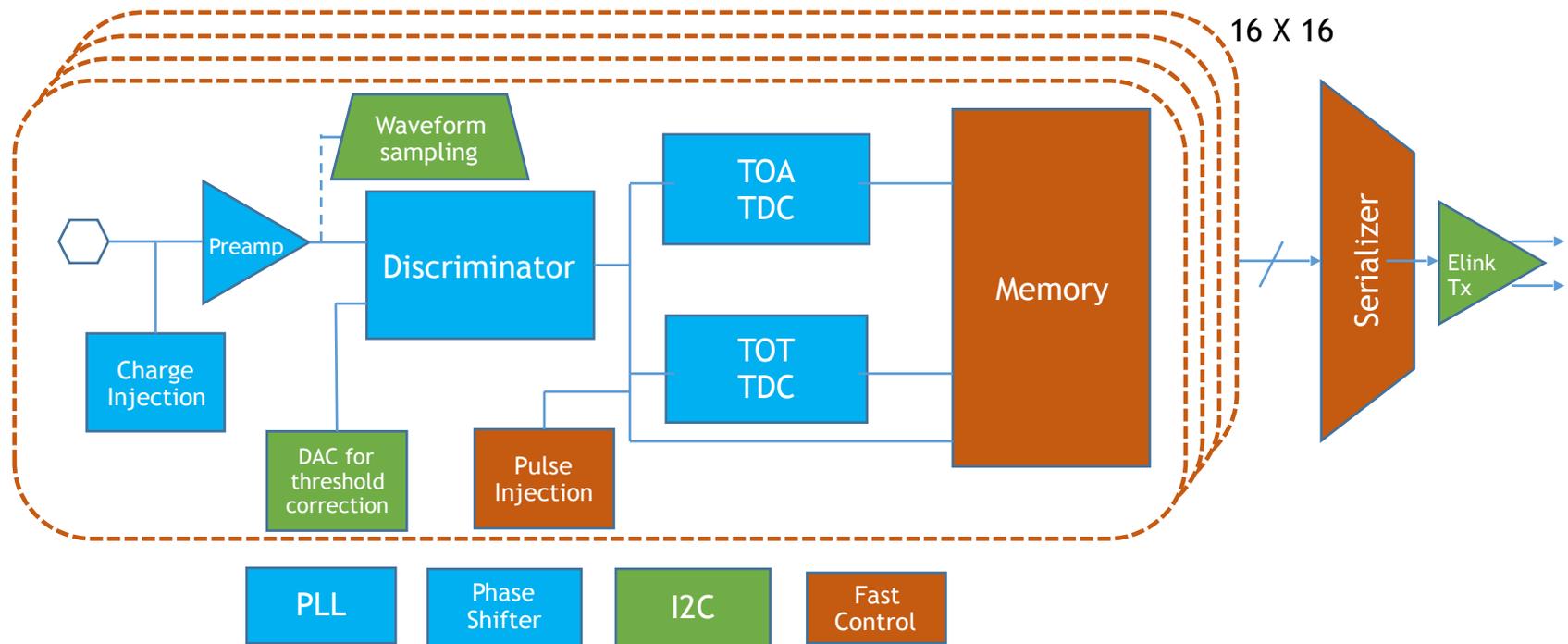
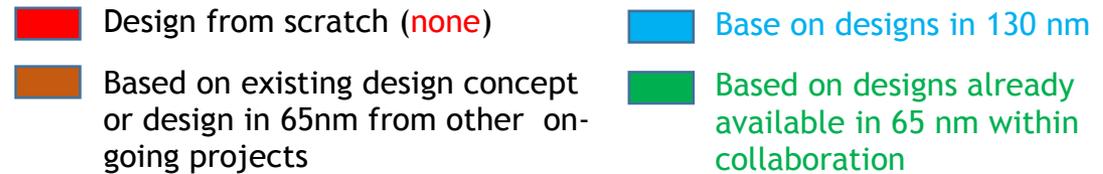
- First prototype submitted in Dec; expected March. Will be used to validate the simulated performance.



- Ted Liu will describe this progress and the full design and prototyping plan in tomorrow's breakout session.

ETL Readout ASIC progress

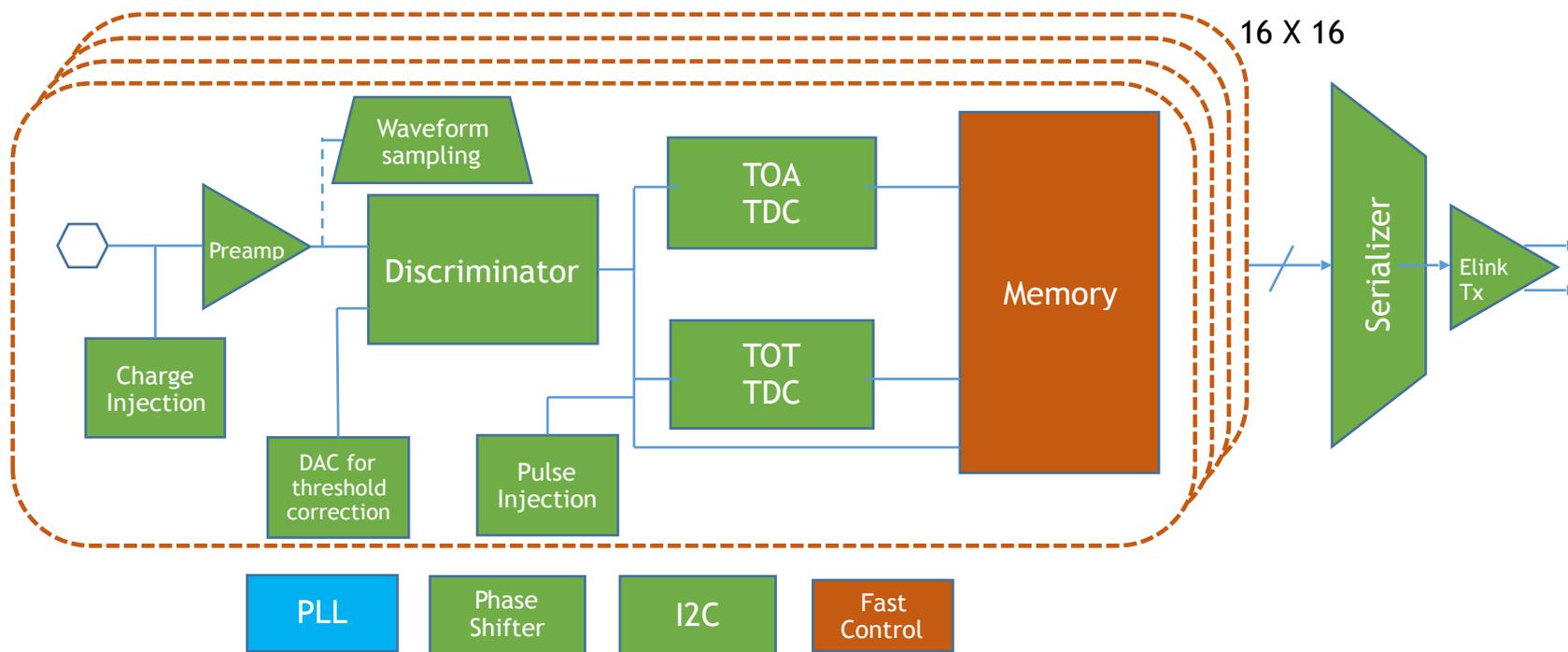
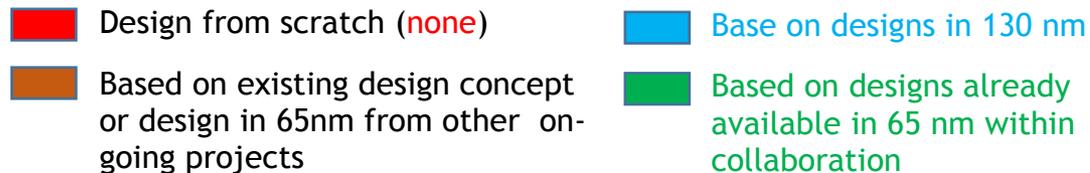
- Design of ETROC1 is progressing well for summer submission.



Beginning status of blocks

ETL Readout ASIC progress

- Design of ETROC1 is progressing well for summer submission.

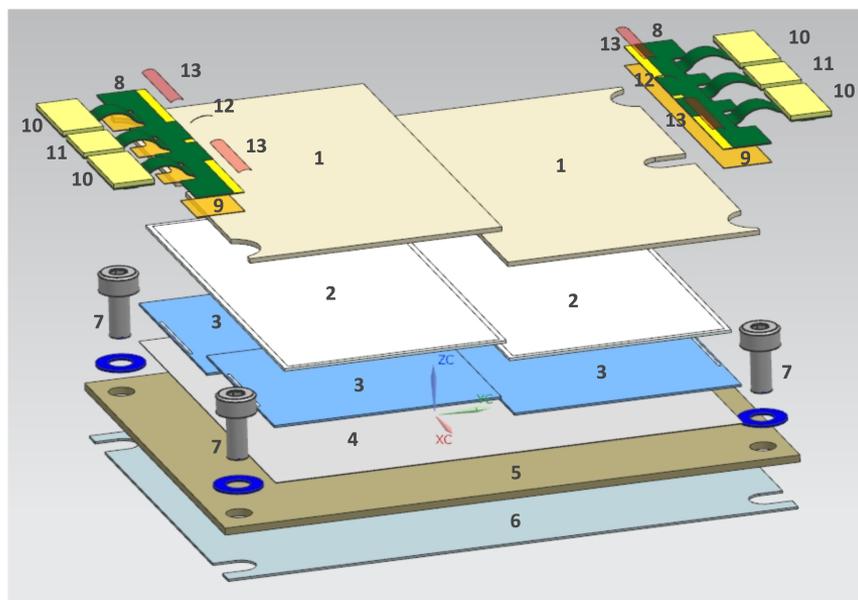


Current status of blocks



ETL Module assembly optimization

- Design, prototyping, and assembly of modules are a significant US CMS deliverable.



- 1: AIN module cover
- 2: LGAD sensor
- 3: ETL ASIC
- 4: Mounting film
- 5: AIN carrier
- 6: Mounting film
- 7: Mounting screw
- 8: Front-end hybrid
- 9: Adhesive film
- 10: Readout connector
- 11: High voltage connector
- 12: LGAD bias voltage wirebond
- 13: ETROC wirebonds

- Assembly plan well developed and documented.
- Elegantly simple; designed to be easily buildable.
(Recent simplification beyond BoE frozen in P6, with small cost savings).
- Details in Frank Golf's talk in tomorrow's breakout.



Design documented: CDR and TDR

- The TDR is now under collaboration review.
- It was seeded by the CDR for the Technical Review.
- The design has been extended from a conceptual to a technical design, with US CMS leadership.
- The updated CDR includes this evolution.

Summary

- Technical review was positive on all charge items:
 - “Current design meets their physics requirements.”
 - “The committee felt that the overall maturity was more advanced than numbers quoted and more than what is required for CD-1. ”
- We have responded to the Technical Review recommendations.
- We have made substantial further progress on the design, the BTL CC, the ETL ASIC, and the ETL module assembly.
- In terms of technical review and documented design, we are ready for CD-1.